1. Claims 1-18 are presented for examination.

2. Figure 14 should be designated by a legend such as --Prior Art-- because only that which is old is illustrated. See MPEP § 608.02(g). Corrected drawings in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

3. Applicants describe Fig. 14 in their Background Art section as follows: "Document 1 (Published Japanese patent application No. 2002-238034) discloses a prior art on a conventional semiconductor device which possesses an interface operable to connect to an external CPU, and performs signal processing of multimedia data, such as image and sound data. Fig. 14 is a block diagram illustrating a conventional semiconductor device 10 for multimedia-data processing. The semiconductor device 10 shown in Fig. 14 is described by the document 1, in which an internal CPU 1, a video processor 2, and an audio processor 3 are connected to a bus 9, and the internal CPU 1 is connected to an external CPU 4 via an interface (not shown). The internal CPU 1 controls the entire semiconductor device 10, the video processor 2 processes a video signal, and the audio processor 3 processes an audio signal. The internal CPU 1 performs processing according to the instructions from the external CPU 4.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

5. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

6. Claims 1-18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Date (Publication No. 2004/0064625) in view of applicants' specification.

7. Date substantially taught the invention of exemplary claim 1 including a semiconductor device (Fig. 1, label which says Chip Boundary) comprising: a processor unit (Fig. 1, CPU Core 0); an internal interface section connected to said processor unit (Fig. 1, System Bus Bridge); an external interface section (Fig. 1, Ext. Bus IF) connected to said processor unit and said internal interface section (Fig. 1, System Bus Bridge connects the external interface element to the CPU Core 0); and a data processing unit (Fig. 1, Memory Management Unit (105)) connected to said internal interface section (Fig. 1, MC Bus, System Bus Bridge), wherein said processor unit

comprises an internal CPU (Fig. 1, CPU Core 0), wherein said external interface section is connected to an external CPU (Fig. 1, CPU Chip (103)), and wherein said data processing unit can be controlled by any one of said internal CPU and the external CPU, via said internal interface section (Fig. 1).

8. Date did not teach a plurality data processing units. However, the prior art Fig. 14 discussed by applicants in their Background Art section makes clear that having a plurality of internal data processing units which are used by both internal and external CPUs was known in the art. The combined teachings make possible a variety of performance levels for systems which can drive internal data processing units by external CPU commands delivered through internal CPUs or by external CPUs directly controlling internal data processing units while bypassing internal CPUs (paragraphs [0024] through [0027]).

9. Claims 2-16 are merely a recitation of different combinations of the same inventive concepts using known components in a manner where the results would be predictable to one of ordinary skill in the art. For example, one can connect internal and external CPUs to the same or different busses (Fig. 1). One can have multiple internal and external CPUs in varied combinations (Fig. 1 of Date shows multiple internal CPUs and the Japanese patent application No. 2002-238034 cited in applicants' Background Art section shows two external CPUs). One can control internal functional units from external CPUs through internal CPUs or bypass the internal CPUs (Fig. 1). Claim 17 is merely for use of the semiconductor device of claim 1 in a mobile phone consisting of prior art devices. The examiner takes Official Notice of the fact that application

processing LSIs; RF processing LSIs; and baseband processing LSIs are conventional components of mobile phones. Using the LSI of applicants' claim 1 in the place of another conventional LSI for processing audio and video data in a modern cell phone is merely substitution with a predictable result. Utilizing multiple CPUs in the application processor, as in claim 18, is merely an extension of the known concept of providing additional processing power as tasks become more complex and numerous. Applicants have taught no new fabrication technology to enable placing multiple CPUs on such a chip. They merely used conventional technology. Otherwise, they would have failed to enable their device if they had used new technology and failed to disclose it.

10. MPEP 2141 reads, in part, as follows:

The Supreme Court in *KSR* reaffirmed the familiar framework for determining obviousness as set forth in *Graham v. John Deere Co.* (383 U.S. 1, 148 USPQ 459 (1966)), but stated that the Federal Circuit had erred by applying the teaching-suggestion-motivation (TSM) test in an overly rigid and formalistic way. *KSR*, 550 U.S. at, 82 USPQ2d at 1391. Specifically, the Supreme Court stated that the Federal Circuit had erred in four ways: (1) "by holding that courts and patent examiners should look only to the problem the patentee was trying to solve" (*Id.* at__ 82 USPQ2d at 1397); (2) by assuming "that a person of ordinary skill attempting to solve a problem will be led only to those elements of prior art designed to solve the same problem" (*Id.*); (3) by concluding "that a patent claim cannot be proved obvious merely by showing that the combination of elements was obvious to try'" (*Id.*); and (4) by overemphasizing "the risk of courts and patent examiners falling prey to hindsight bias" and as a result applying "[r]igid preventative rules that deny factflnders recourse to common sense" (*Id.*).

In *KSR*, the Supreme Court particularly emphasized "the need for caution in granting a patent based on the combination of elements found in the prior art," *Id*, at__82 USPQ2d at 1395, and discussed circumstances in which a patent might be determined to be obvious. Importantly, the Supreme Court reaffirmed principles based on its precedent that "the combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. "*Id*, at__82 USPQ2d at 1395.

11. The Supreme Court further stated that:

> When a work is available in one field of endeavor, design incentives and other market forces can prompt variations of it, either in the same field or a different one. If a person of ordinary skill can implement a predictable variation, § 103 likely bars its patentability. For the same reason, if a technique has been used to improve one device, and a person of ordinary skill in the art would recognize that it would improve similar devices in the same way, using the technique is obvious unless its actual application is beyond his ordinary skill. *Id*. at__82 USPQ2d at 1396. When considering obviousness of a combination of known elements, the operative question is thus "whether the improvement is more than the predictable use of prior art elements according to their established functions." *Id*. at__82 USPQ2d at 1396.

12. All the elements necessary to produce applicants' invention were known in the art. How one combined such elements to produce applicants' invention was also known in the art. Evidence of this is that applicants' disclosure lacks any detailed description of the circuitry necessary to implement applicants' invention. One of ordinary skill would have readily recognized that the results of the combination were predictable. Absent some secondary considerations, not in evidence at this time, applicants invention is obvious over the combination of prior art presented.

13. To assist applicants should they chose to challenge the examiner's Official Notice, the examiner is pointing out that following the KSR decision by the Supreme Court, the Office has changed its policy related to Official Notice. The Office now requires applicants to provide persuasive evidence and/or arguments directly refuting the Official Notice before a supporting reference is to be supplied by the examiner.

14. Any inquiry concerning this communication should be directed to William M. Treat at telephone number (571) 272-4175.

15. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

/William M. Treat/
Primary Examiner, Art Unit 2181